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April 2, 2001

Via Registered Mail
Return Receipt Requested

Mr. Christopher E. Phillips
5888 Assis Court
San Jose, CA 95138

Re: U.S. Patent Application Serial No. 09/679,398
Filed: October 3, 2000
For: HIERARCHICAL STORAGE ARCHITECTURE FOR RECONFIGURABLE LOGIC CONFIGURATIONS
Our Reference: 032001-011

Dear Mr. Phillips:

We represent Chameleon Systems, Inc.

Enclosed is a copy of the Notice to File Missing Parts from the U.S. Patent and Trademark Office dated November 29, 2000, to which a response was due on January 29, 2001, with an extendable deadline of April 29, 2001, with extension fees. Enclosed for signature is an Assignment, and a Combined Declaration and Power of Attorney. We have previously sent you copies of these papers on December 14, 2000, and February 1, 2001. As required by your employee agreement with Chameleon, please sign these papers where indicated, and return them to me for filing in response to the Notice to File Missing Parts of Application by April 20, 2001. Duplicate originals of these papers have also been sent to Dale Wong for signature.

For your convenience, I am enclosing a copy of the above-referenced application as filed in the U.S. Patent and Trademark Office on October 3, 2000.

Please contact me if you have any questions.

Sincerely yours,

Joseph P. O'Malley

JPO:mms
Enclosures
c: Scott Plamondon (w/o enc.)
c: Robert E. Krebs (w/o enc.)

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032001-011

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

Hierarchical Storage Architecture for Reconfigurable Logic Configurations

the specification of which

(check one)
- ☐ is attached hereto;
- ☒ was filed on October 3, 2000 as

Application No. 09/679,398

and was amended on _____; (if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032001-011

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

William L. Mathis	17,337	Eric H. Weisblatt	30,505	Bruce T. Wieder	33,815
Robert S. Swecker	19,885	James W. Peterson	26,057	Todd R. Walters	34,040
Platon N. Mandros	22,124	Teresa Stanek Rea	30,427	Ronni S. Jillions	31,979
Benton S. Duffett, Jr.	22,030	Robert E. Krebs	25,885	Harold R. Brown III	36,341
Norman H. Stepno	22,716	William C. Rowland	30,888	Allen R. Baum	36,086
Ronald L. Grudziecki	24,970	T. Gene Dillahunty	25,423	Steven M. duBois	35,023
Frederick G. Michaud, Jr.	26,003	Patrick C. Keane	32,858	Brian P. O'Shaughnessy	32,747
Alan E. Kopecki	25,813	B. Jefferson Boggs, Jr.	32,344	Kenneth B. Leffler	36,075
Regis E. Slutter	26,999	William H. Benz	25,952	Fred W. Hathaway	32,236
Samuel C. Miller, III	27,360	Peter K. Skiff	31,917	Wendi L. Weinstein	34,456
Robert G. Mukai	28,531	Richard J. McGrath	29,195	Mary Ann Dillahunty	34,576
George A. Hovanec, Jr.	28,223	Matthew L. Schneider	32,814		
James A. LaBarre	28,632	Michael G. Savage	32,596		
E. Joseph Gess	28,510	Gerald F. Swiss	30,113		
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21839

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Address all telephone calls to: Joseph P. O'Malley at (650)622-2300.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
CHRISTOPHER E. PHILLIPS		
RESIDENCE	CITIZENSHIP	
5888 Assis Court, San Jose, CA 95138	United States of America	
POST OFFICE ADDRESS		
5888 Assis Court, San Jose, CA 95138		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY	SIGNATURE	DATE
DALE WONG		
RESIDENCE	CITIZENSHIP	
855 35th Avenue, San Francisco, CA 94121	United States of America	
POST OFFICE ADDRESS		
855 35th Avenue, San Francisco, CA 94121		

032001-011
Attorney's Docket No.

ASSIGNMENT
(JOINT)

THIS ASSIGNMENT, by CHRISTOPHER E. PHILLIPS, and DALE WONG, residing at 5888 Assisi Court, San Jose, California 95138-2314 and 855 35th Avenue, San Francisco, California 94121 (hereinafter referred to as "the Assignors"), respectively, witnesseth:

WHEREAS, the Assignors have invented certain new and useful improvements in HIERARCHICAL STORAGE ARCHITECTURE FOR RECONFIGURABLE LOGIC CONFIGURATIONS, set forth in an application for Letters Patent of the United States,

(1) ☐ which is a provisional application
  (a) ☐ to be filed herewith; or
  (b) ☐ bearing Application No. __, and filed on _; or

(2) ☒ which is a non-provisional application
  (a) ☐ having an oath or declaration executed on even date herewith prior to filing of application;
  (b) ☒ bearing Application No. 09/679,398, and filed on October 3, 2000; or
  (c) ☐ to be filed; and

WHEREAS, CHAMELEON SYSTEMS, INC.,, a corporation duly organized under and pursuant to the laws of THE STATE OF CALIFORNIA and having its principal place of business at 161 NORTECH PARKWAY, SAN JOSE, CA 95134 (hereinafter referred to as "the Assignee"), is desirous of acquiring the entire right, title, and interest in and to said inventions, the right to file applications on said inventions and the entire right, title and interest in and to any applications, including provisional applications for Letters Patent of the United States or other countries claiming priority to said application, and in and to any Letters Patent or Patents, United States or foreign, to be obtained therefor and thereon.

NOW, THEREFORE, in consideration of One Dollar ($1.00) and other good and sufficient consideration, the receipt of which is hereby acknowledged, the Assignors have sold, assigned, transferred, and set over, and by these presents do sell, assign, transfer, and set over, unto the Assignee, its successors, legal representatives, and assigns the entire right, title, and interest in and to the above-mentioned inventions, the right to file applications on said inventions and the entire right, title and interest in and to any applications for Letters Patent of the United States or other countries claiming priority to said applications, and any and all Letters Patent or Patents of the United States of America and all foreign countries that may be granted therefor and thereon, and in and to any and all applications claiming priority to said applications, divisions, continuations, and continuations-in-part of said applications, and reissues and extensions of said Letters Patent or Patents, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by the Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives, and assigns, to the full end of the term or terms for which Letters Patent or Patents may be granted as fully and entirely as the same would have been held and enjoyed by the Assignors had this sale and assignment not been made;

AND for the same consideration, the Assignors hereby covenant and agree to and with the Assignee, its successors, legal representatives, and assigns, that, at the time of execution and delivery of these presents, the Assignors are the sole and lawful owners of the entire right, title, and interest in and to the inventions set forth in said applications and said applications, including provisional applications, above-mentioned, and that the same are unencumbered, and that the Assignors have good and full right and lawful authority to sell and convey the same in the manner herein set forth;

AND for the same consideration, the Assignors hereby covenant and agree to and with the Assignee, its successors, legal representatives, and assigns that the Assignors will, whenever counsel of the Assignee, or the counsel of its successors, legal representatives, and assigns, shall advise that any proceeding in connection with said inventions or said applications for Letters Patent or Patents, or any proceeding in connection with Letters Patent or Patents for said inventions in any country, including interference proceedings, is lawful and desirable, or that any application claiming priority to said application, division, continuation, or continuation-in-part of any applications for Letters Patent or Patents, or any reissue or extension of any Letters Patent or Patents to be obtained thereon, is lawful and desirable, sign all papers and documents, take all lawful oaths, and do all acts necessary or required to be done for the procurement, maintenance, enforcement, and defense of Letters Patent or Patents for said inventions, without charge to the Assignee, its successors, legal representatives, and assigns, but at the cost and expense of the Assignee, its successors, legal representatives, and assigns;

AND the Assignors hereby authorize and request the attorneys of BURNS, DOANE, SWECKER & MATHIS, L.L.P. of Alexandria, Virginia to insert in the spaces provided above the filing date, application number, and attorney docket number of said application when known.

AND the Assignors hereby request the Commissioner of Patents to issue any and all said Letters Patent of the United States to the Assignee as the Assignee of said inventions, the Letters Patent to be issued for the sole use and behalf of the Assignee, its successors, legal representatives, and assigns.

Date_____ Signature of Assignor _____
Christopher E. Phillips

Date_____ Signature of Assignor _____
Dale Wong

PATENT
ATTORNEY'S DOCKET NO. 032001-011

"Express Mail" Mailing Label No. EL 521 508 415 US
Date of Deposit October 3, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, with sufficient postage affixed, and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

Seini Matangii
(Typed or printed name of person mailing paper or fee)

HIERARCHICAL STORAGE ARCHITECTURE FOR RECONFIGURABLE LOGIC CONFIGURATIONS

ABSTRACT OF THE DISCLOSURE

1. Field of the Invention

The present invention relates to reconfigurable computing.

2. State of the Art

A Field Programmable Gate Array (FPGA) is a single-chip combination of computing elements and storage elements. The computing elements can be configured to implement different logic functions depending on the values stored in the storage elements. A collection of such values that can configure all the computing elements on the chip will be referred to as a "configuration plane". A collection of values that is a subset of a plane will be referred to as a "configuration."

In a conventional FPGA, there is only enough on-chip storage for a single configuration plane. In a variant of FPGAs known as Reconfigurable Logic, there may be enough on-chip storage for multiple configuration planes. In reconfigurable logic there is typically some mechanism for rapidly changing which plane is currently configuring the computing elements. In addition, there is typically some mechanism for loading the multiple planes from off-chip storage, which can result

in virtually unlimited configurations for the chip. However, the time required to load the off-chip configuration data is the bottleneck for current implementations.

The off-chip loading is typically handled by either a caching or a pre-fetch strategy. In a caching strategy, an on-chip cache of the most recently used configurations is stored, and in the event of a cache miss, the chip is stalled until the configuration can be loaded from off-chip. This is a delay of several hundreds of clock cycles for the current generation of reconfigurable logic. In a pre-fetch strategy, the overall schedule of configuration invocations is analyzed and the appropriate configurations are loaded into the configuration planes before they are needed, ideally avoiding stalling the chip. However, the more time required to load an off-chip configuration, the more branching in the configuration schedule will be encountered between the pre-fetch and the actual use, possibly invalidating the original pre-fetch decision and stalling the chip.

SUMMARY OF THE INVENTION

The present invention, generally speaking, provides a hierarchy of configuration storage. The highest level of the hierarchy is an active configuration store; the lowest level is an off-chip configuration store; in between are one or more levels of configuration stores. Every configuration is promoted from the lowest off-chip level, through each level, up to the highest active level. Each ascending level of the hierarchy has a decreasing latency time required to promote a configuration to the next higher level of the hierarchy, and a decreasing amount of available storage. This separation into levels allows the amount of available storage to be adjusted depending on the inherent latency of the level's storage mechanism, where a longer latency requires a larger cache. This in turn allows the total required storage for a given performance level to be minimized.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended ~~drawing~~. In the drawing:

Figure 1 is a diagram of an exemplary configuration storage hierarchy;

Figure 2a is a simplified example of a configuration to be compressed;

Figure 2b is a compressed format used to represent the configuration of Figure 2a, the bits of the representation being further compressed;

Figure 3 is a diagram showing an example of a suitable on-chip cache;

Figure 4 is a diagram showing an example of decompression;

Figure 5 is a diagram showing an example a of planes/configuration table;

Figure 6a is a block diagram of a portion of a memory plane stack;

Figure 6b is a diagram of a group of corresponding memory cells, one cell form each plane of the memory stack of Figure 6a;

Figure 6c is a diagram of an alternative embodiment of the memory stack of Figure 6a in which separate "function" and "wire" stacks are provided;

Figure 6d is a diagram of separate memory stacks provided for control, datapath and memory configuration, respectively;

Figure 6e is a diagram of a common memory stack provided for control, datapath and memory configuration; and

Figure 7 is a schematic diagram of an alternative embodiment for a single bit of the memory stack of Figure 6a.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 1, in a preferred embodiment of the present invention, an FPGA or reconfigurable logic device is provided with a configuration storage hierarchy having multiple levels, e.g., four levels: 1) off-chip storage, 2) compressed cache storage, 3) decompressed configuration planes, and 4) one or more active configuration planes. A description of each level follows, proceeding from lowest to highest level.

Off-Chip

The off-chip level of storage may be implemented in a variety of technologies, including without limitation EEPROM, RAM, hard drive, or I/O port. Preferably, the external storage device is memory mapped (corresponds to address entry in system CPU memory access space), and an instruction to load a specific configuration from off-chip storage device will include the configuration's starting address and length. The length of a configuration will vary depending on: how many computing elements it configures, the specific function for each computing element, and the amount of compression achieved.

A configuration may include an arbitrary number of computing and/or routing elements. Nor is there any restriction that the elements be contiguous on the chip. Partial reconfiguration may be used to support a "data-in-place" computing style where some computing elements configured as registers and holding active data are left untouched, while other computing elements are reconfigured to perform new functions on the data. Partial reconfiguration may be performed. For "data in place," storage contents are left in place at either/or register and local memory elements. The control logic or wiring interconnectivity can be updated with new certification data while the rest of the configuration data fields for the storage remains unchanged. In a preferred embodiment, routing between elements can remain static while the control codes are updated. In both of these cases, selected

subsets of configurations are used, resulting in effective benefits of partial reconfiguration.

The off-chip configurations are stored in a compressed format. One possible compression scheme is described here. Referring to Figure 2a, the computing elements on the chip are in a two dimensional X and Y array. A computing element is configured by storing an opcode (e.g., 1, 3, 7, etc.) in the computing element. Routing elements occupy rows and columns where all elements in a row have the same Y coordinate, and all elements in a column have the same X coordinate. Referring to Figure 2b, a single configuration consists of a series of instructions, to be executed in sequence, all with the following three-field format: Y control, X control, opcode. The Y control is a binary number from 0 to N-1, where N is the maximum possible Y coordinate. The X control is an N bit wide word, where N is the maximum possible X coordinate. In other words, the X control has one bit for every column, and the Y control is decoded for each row. In the row enabled by the Y control, for each element in the row where the corresponding X control bit is a 1, the specified opcode will be loaded into the element. On top of this "common configuration" compression, the entire configuration (sequence of instructions) may be bit-wise run length compressed.

In an alternative implementation, the Y control may not be encoded if the savings from simultaneously loading multiple rows with the same opcode outweighs the savings from encoding the row coordinate.

In addition to being compressed, the configurations may also be encrypted.

The number of bits used to configure a single element may vary. It is possible to apply, for example, Huffman encoding to the set of possible configuration codes so that the more frequently used codes require fewer bits than the less frequently used codes. Even if a fixed bit-width is used for the opcode, maximizing the number of leading zeros will help in a run length compression scheme.

Compressed Cache

The on-chip compressed cache can be loaded directly from the off-chip configurations. The on-chip cache has its own dedicated DMA server. The configurations are loaded directly from off-chip without any modification, in compressed format. As a result, more configurations can be stored in a given amount of cache, and the off-chip loading time is minimized.

Referring to Figure 3, one possible implementation of the cache is as follows. The on-chip compressed cache may be implemented as a RAM with multiple cache "lines", where each line consists of a configuration field, a contents addressable field, and a tagged bit field. The contents addressable field will store the address of the configuration, which is the same as the off-chip address used to load the configuration. The tagged bit field is used during a search of the cache for a given configuration. The tag bit is set to TRUE for any line with an address field that exactly matches a searched for address, and is set to FALSE otherwise. Whenever a configuration is loaded into the cache, a search is performed first to check if there is already a line with the same address. If so, the off-chip configuration is loaded on top of the existing line in the cache. If not, the first available line is used. A separate counter with wrap around is maintained to indicate the first available line. If the first available line's address field is not equal to zero, an error flag is raised. When a line in the cache is freed, its address field is set to zero. Instead of a wrap around counter, an alternate method for identifying an available line is to search for a zero address and use the first available.

Decompressed Planes

The decompressed planes are loaded with configurations from the compressed cache, with stream-oriented decompression and decoding. Once they are in the decompressed planes, configurations can be moved into the active plane in

as little as a single clock cycle. The decompressed planes serve as the rapid staging area for the active plane.

Referring to Figure 4, one possible implementation of the decompression and decoding process is as follows. A fixed bit-width is assumed for the length field of the run-length compressed bitstream. The length field value is loaded into a count down counter. The next bit is shifted into a shift register until the counter reaches zero or the register is filled. The bit-width of the register corresponds to the length of a single configuration instruction. The instruction's X, Y, and opcode fields will have been zero-filled so that the fields are always the same bit-width. When the register is filled, the fields will drive the loading of the decompressed plane accordingly. The process continues until a length field of zero is encountered.

If the configuration instructions are encrypted, they will be decrypted after each configuration instruction is decompressed. In this case, local hardware would intervene to perform the decryption before the disbursement in the configurable storage planes.

Referring to Figure 5, a separate table is maintained that stores the address of the configuration that is currently loaded in each decompressed plane. While the chip is executing, this table can be used to verify that the intended configurations have actually been pre-fetched and are still resident in the planes. This table can also be used to save and restore the state of the chip in the event of an interrupt. This table can also be used to boot some initial configurations into the chip during power-up.

Active Plane

The active plane can be loaded from any of the decompressed planes. A particular embodiment of a memory plane stack 1200 is shown in Figure 6a. In the illustrated example, the top two planes 1206, 1205 of the memory plane stack are configuration planes. Configuration data stored in these planes is applied to the

reconfigurable logic. In the illustrated embodiment, "function" configuration data and "wire" configuration data is stored in different planes. The bottom memory plane 1200a provides external access to the memory stack. Intermediate planes function, for example, as a configuration stack, storing configurations expected to be used by not presently active. In an exemplary embodiment, memory plane 0 is single port, for single-channel read and write between system memory and configuration storage. The remaining memory planes are dual port, having one read port and one write port. Dual port supports simultaneous loading and recirculation of configuration data with the local "stack." If no data compression is used, then simultaneous real-time monitoring is possible, e.g., by writing out a "snapshot" of one or more planes of the stack.

A group of corresponding memory cells, one cell from each plane of the memory stack, is shown in Figure 6b. The ports of all of the cells are interconnected so as to allow an operation in which the contents of a cell within any plane may be read and then written to the corresponding cell of any other plane. For example, by activating the appropriate control signal, the contents of plane 4 may be read and written into plane 6. Such an operation may be accomplished, preferably, in a single clock cycle, or at most a few clock cycles. Configuration data is loaded from external main memory into plane 0 of the memory stack in anticipation of its being transferred into a configuration plane.

Alternatively, separate "function" and "wire" stacks may be provided, as shown in Figure 6c. Using this arrangement, function and wire configurations may be changed simultaneously. Similarly, configuration stacks for configuration of control, datapath and memory may be combined (Figure 6d) or separate (Figure 6e).

A schematic diagram of an alternative embodiment of a cell stack is shown in Figure 7, showing a cross section of several configuration planes 1301-1304 and the lockable fabric-definition cell 1305 that produces a Fabric_Define_Data bit for a

single bit location. These bits are aggregated in order to form sufficient bit numbers for functional cell type definition. For instance, a four bit grouping might designate between four to sixteen different cell type definitions. The other latch sites below the storage cell are for additional configuration plane data available for swapping as needed by functional scheduling requirements. These storage locations can be written and read to from a common configuration data bus structure. The Config_Read_Data and Config_Load_Data buses 1307 and 1309, although shown as being separate, can be combined as a single bi-directional bus for wiring efficiency. This bus structure allows configuration data to be written as needed. The Swap_Read_Plane buffer 1311 allows existing configuration plane data contents to be swapped among differing configuration planes on a selectable basis. For instance, the current operation plane of data can be loaded from configuration plane 1 to configuration plane 2 by the use of the Swap_Read_Plane buffer 1311. The structure shown in Figure 7 is similar to a conventional SRAM memory structure which allows a dense VLSI circuitry implementation using standard memory compiler technology. This structure could also be implemented as a conventional dual port RAM structure (not shown) which would allow for concurrent operation of the write and read data operations. Unlike Figure 6b, the example of Figure 7 assumes separate configuration stacks for each configuration plane as described hereinafter. That is, the bit stack produces only a single Fabric_Define_Data bit instead of multiple fabric definition data bits as in Figure 6b. The bits could also be extended to include registers operating in a like fashion.

If the Data_Recirc_Read line 1313 is also connected to data storage locations that are used for normal circuit register operation, then real time monitoring of device operations can be utilized by the operating system for applications such as RMON in internetworking application area or for real time debug capability. The RMON application basically uses counter operation status from registers in order to determine system data operation flow characteristics.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is claimed is:

1. A hierarchy of logic configuration storage, the hierarchy consisting of at least external storage, on-chip compressed cache, on-chip decompressed planes, and one or more active planes.

2. A method of configuration of an array of computing and/or interconnect elements, comprising:

decoding configuration memory by rows and columns; and

applying configuration codes to intersections of selected rows and columns, including a multiplicity of such intersections for the same configuration code.

3. The method of Claim 2, further comprising overwriting an existing configuration code with a new code, allowing the efficient compression of regular arrays with differing end conditions such as configurations of different sizes and differing contents for items of configuration.

4. The method of Claim 3, further comprising:

changing at least some of a computing element's configuration;

holding fixed at least some of a storage element's configuration;

whereby data-in-place reconfiguration is achieved.

5. A reconfigurable computing chip comprising an on-chip configuration cache containing a multiplicity of stored configurations, wherein each configuration is identified by a unique off-chip address used to fetch that configuration.

6. The apparatus of Claim 5, where each configuration is compressed.

7. The apparatus of Claim 5, where the identification of the addresses is performed using contents-addressable memory.

8. In a reconfigurable computing system including a reconfigurable computing chip having reconfigurable logic and multiple configuration planes, the system further including off-chip storage, a method of configuration management, comprising storing in a table a current state of the on-chip configurations, said table consisting of multiple entries, each entry identifying an on-chip configuration plane and identifying a unique off-chip address of a loaded configuration.

9. The method of Claim 8, further comprising:

saving the table, thereby saving the entire state of the reconfigurable logic;

loading the table; and

from information stored in the table, loading the identified configurations into the identified on-chip planes.

10. The method of Claim 8, further comprising establishing initial boot conditions in the reconfigurable logic by:

specifying in the table an address of a boot configuration; and

automatically loading the boot configuration into the reconfigurable computing chip on boot up.

ABSTRACT OF THE DISCLOSURE

The present invention, generally speaking, provides a hierarchy of configuration storage. The highest level of the hierarchy is an active configuration store; the lowest level is an off-chip configuration store; in between are one or more levels of configuration stores. Every configuration is promoted from the lowest off-chip level, through each level, up to the highest active level. Each ascending level of the hierarchy has a decreasing latency time required to promote a configuration to the next higher level of the hierarchy, and a decreasing amount of available storage. This separation into levels allows the amount of available storage to be adjusted depending on the inherent latency of the level's storage mechanism, where a longer latency requires a larger cache. This in turn allows the total required storage for a given performance level to be minimized.

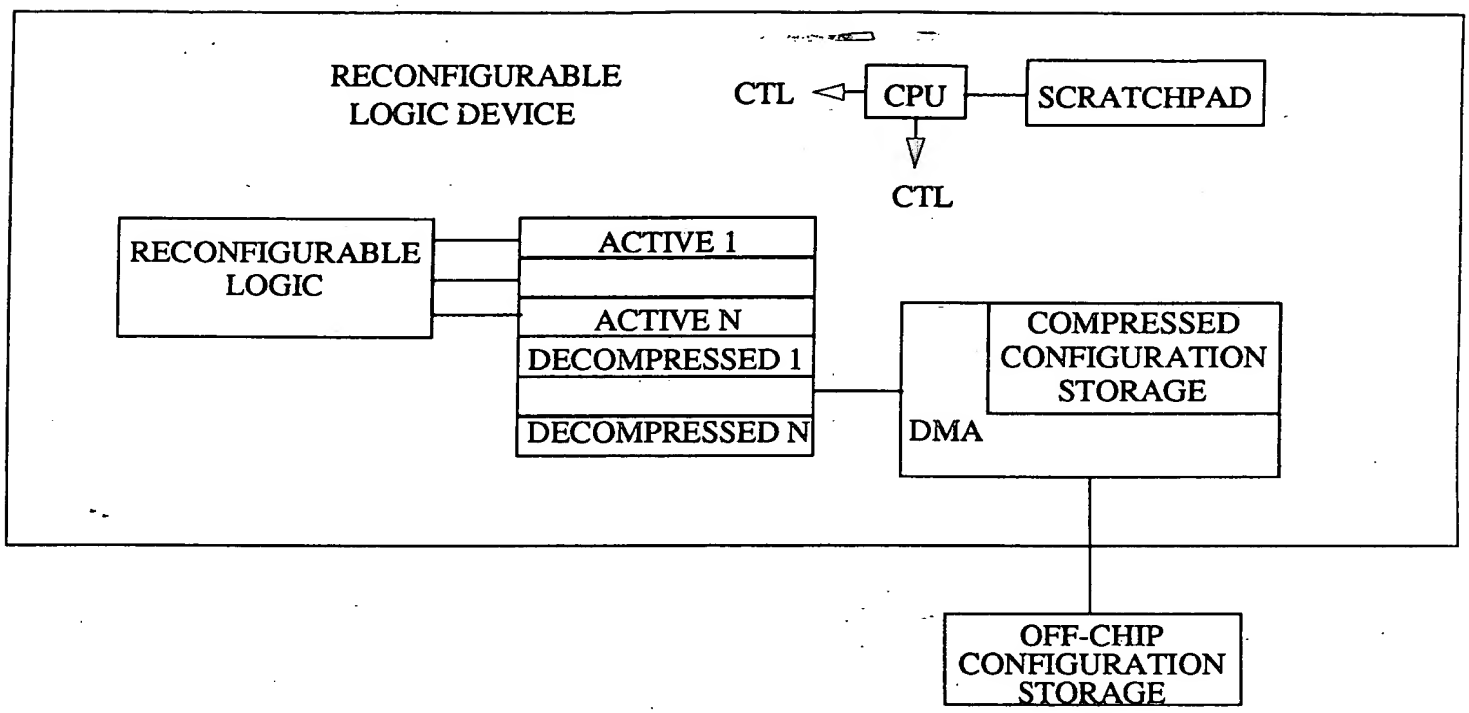
RECONFIGURABLE
LOGIC DEVICE
CTL
CPU
SCRATCHPAD
CTL
RECONFIGURABLE
LOGIC
ACTIVE 1
ACTIVE N
DECOMPRESSED 1
DECOMPRESSED N
COMPRESSED
CONFIGURATION
STORAGE
DMA
OFF-CHIP
CONFIGURATION
STORAGE

Fig. 1

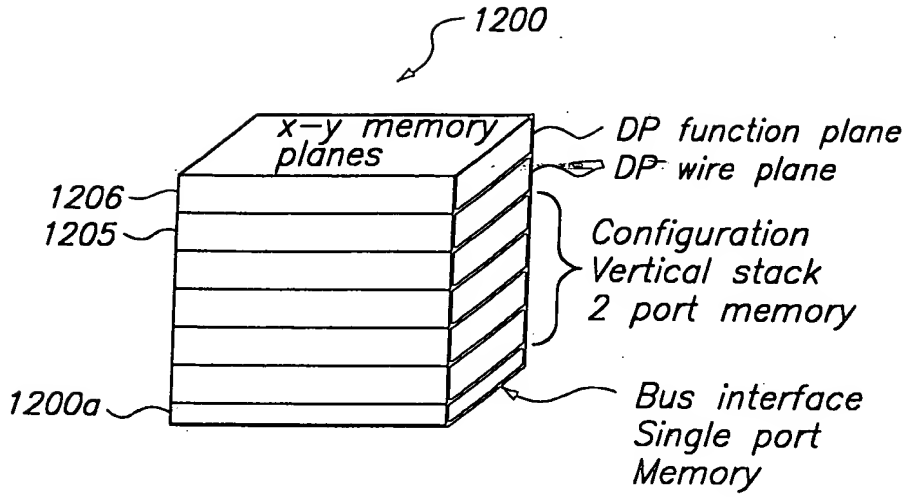
1200
x–y memory planes
DP function plane
DP wire plane
1206
1205
Configuration Vertical stack 2 port memory
1200a
Bus interface Single port Memory

FIG. 6a

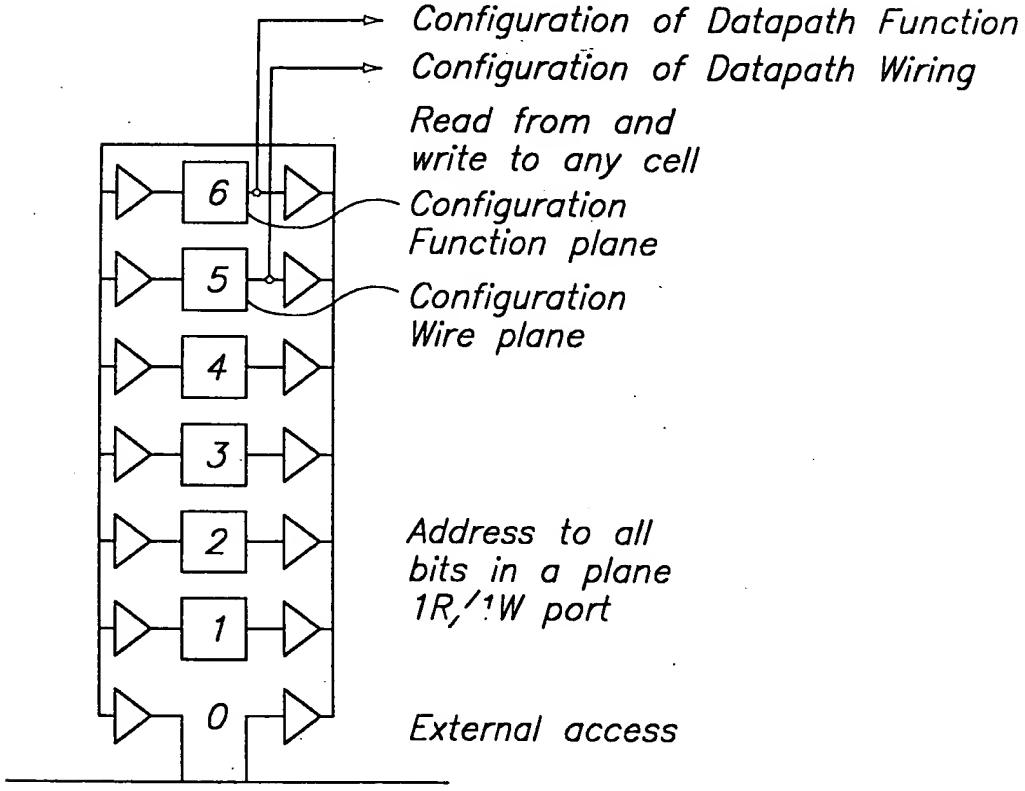
Configuration of Datapath Function
Configuration of Datapath Wiring
Read from and write to any cell
6
5
4
3
2
1
0
Configuration Function plane
Configuration Wire plane
Address to all bits in a plane 1R/1W port
External access

FIG. 6b

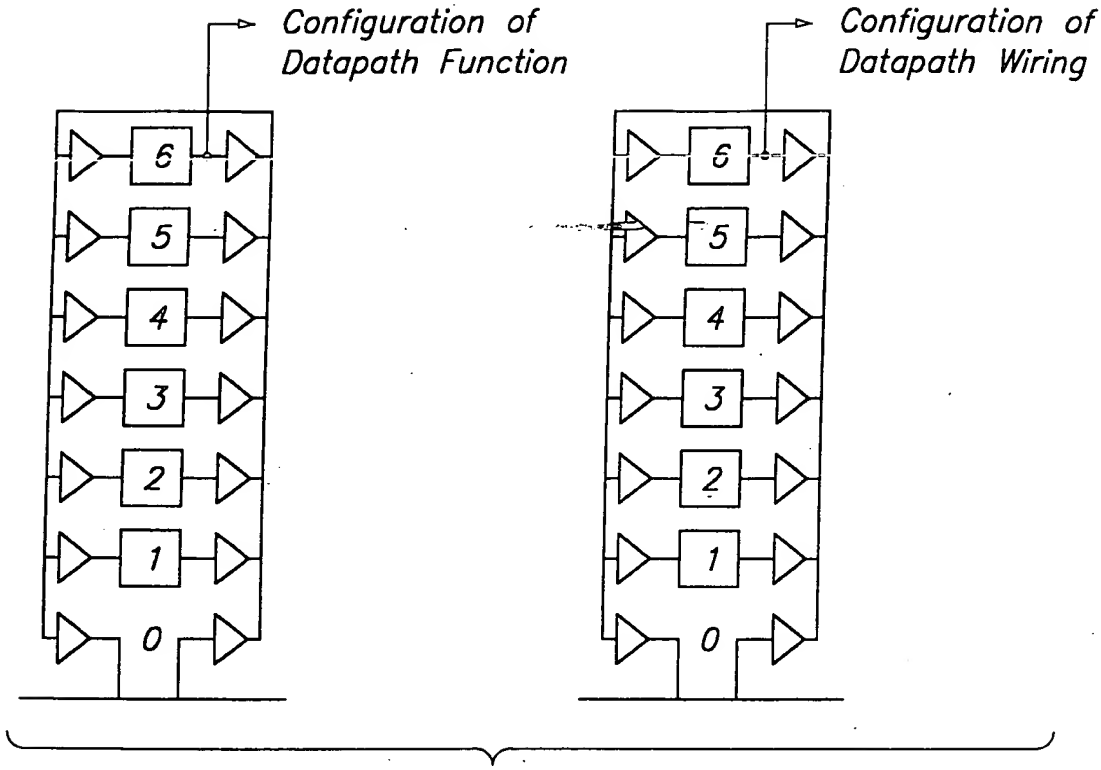
Configuration of Datapath Function
Configuration of Datapath Wiring
6
5
4
3
2
1
0
6
5
4
3
2
1
0

FIG. 6c

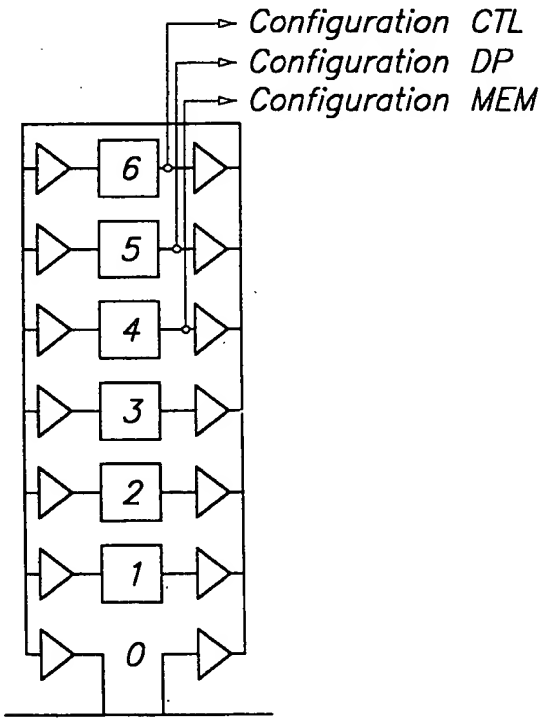
Configuration CTL
Configuration DP
Configuration MEM
6
5
4
3
2
1
0

FIG. 6d

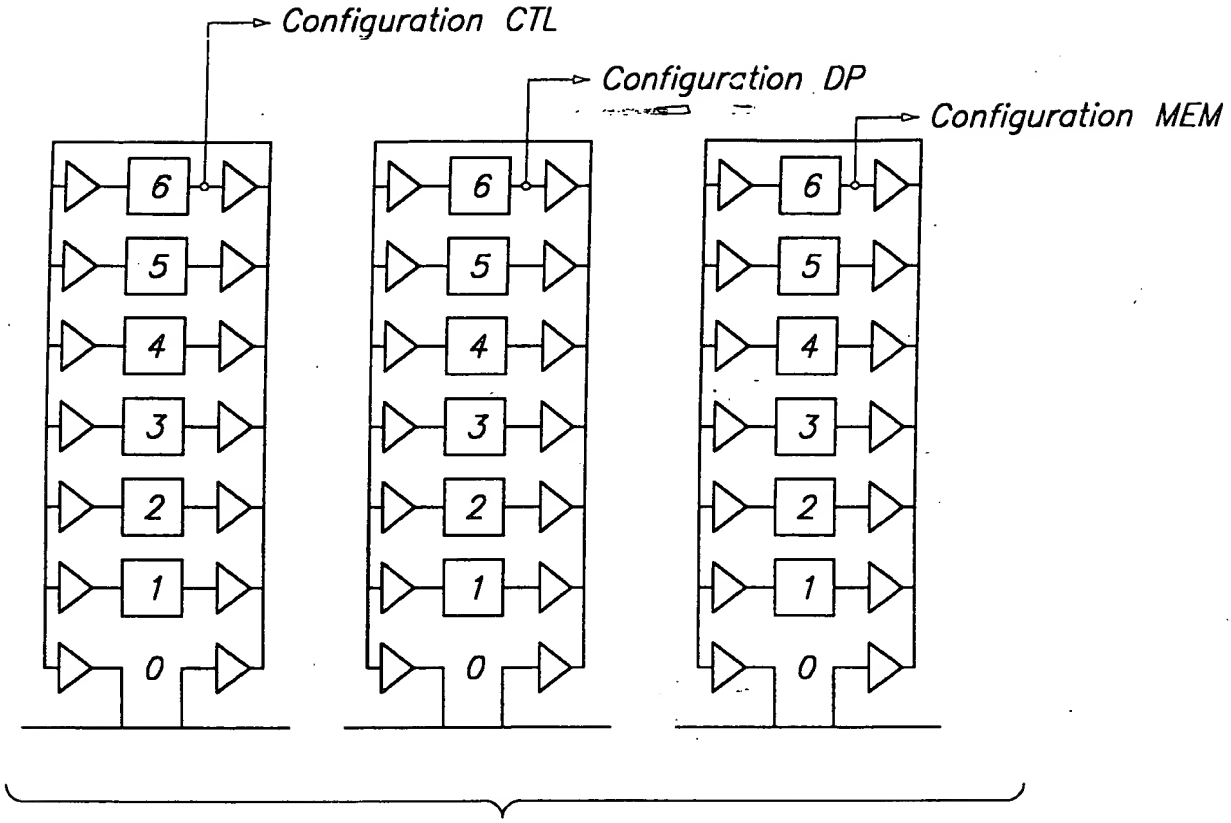
Configuration CTL
Configuration DP
Configuration MEM
6
5
4
3
2
1
0
6
5
4
3
2
1
0
6
5
4
3
2
1
0

FIG. 6e

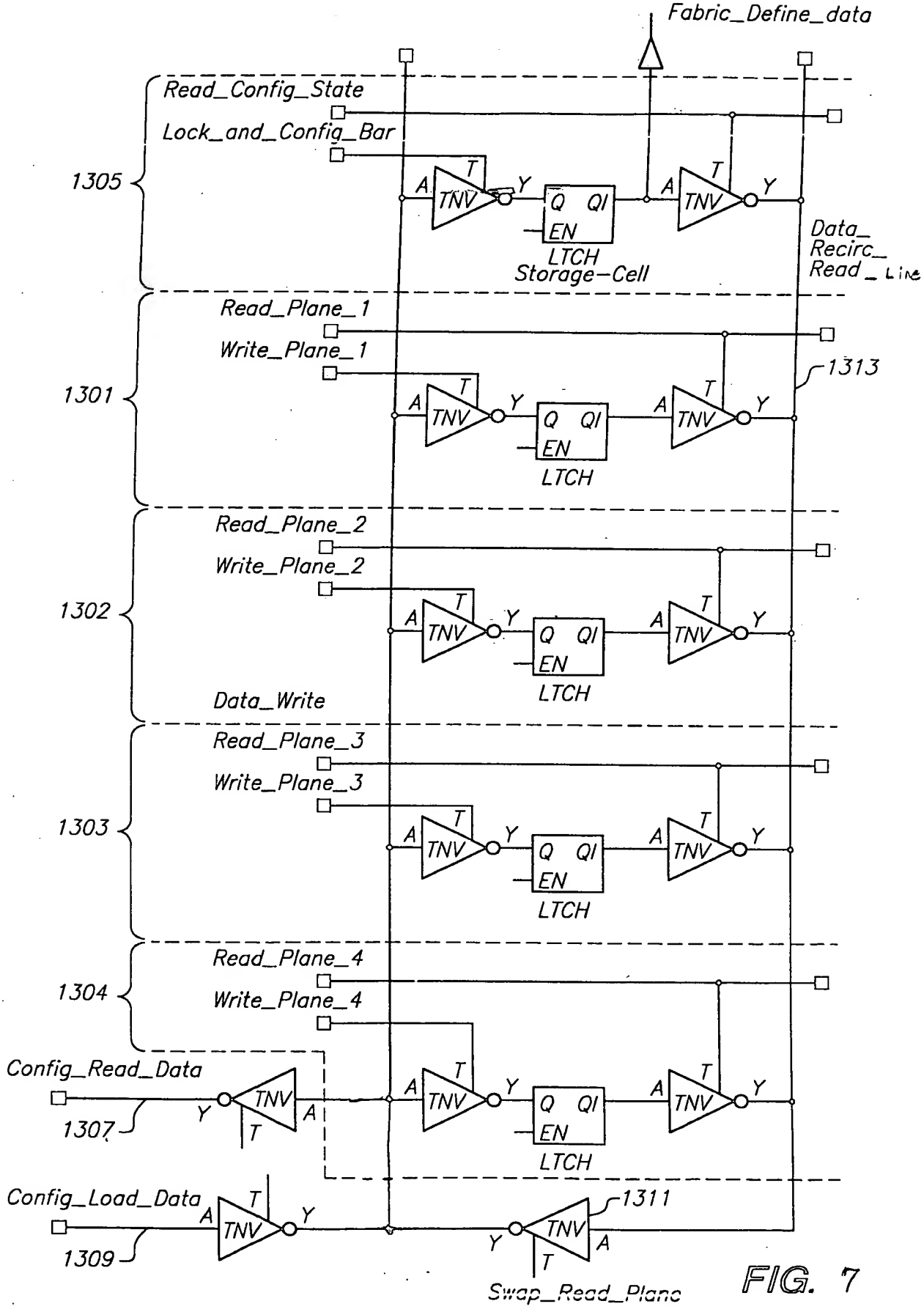
Fabric_Define_data
Read_Config_State
Lock_and_Config_Bar
1305
T
A
TNV
Y
Q QI
EN
LTCH
Storage-Cell
Data_
Recirc_
Read_Line
Read_Plane_1
Write_Plane_1
1313
1301
Read_Plane_2
Write_Plane_2
1302
Data_Write
Read_Plane_3
Write_Plane_3
1303
Read_Plane_4
Write_Plane_4
1304
Config_Read_Data
1307
Config_Load_Data
1309
1311
Swap_Read_Plane

FIG. 7